IN THE CLAIMS:

1. (Currently Amended) A method of forming a vertical double gate semiconductor device comprising:

providing a semiconductor substrate;

providing a first insulating layer over the semiconductor substrate;

providing a first semiconductor layer over the first insulating layer;

removing portions of the first semiconductor layer to form a semiconductor structure having a first sidewall and a second sidewall, wherein the first sidewall is opposite the second sidewall;

forming a second insulating layer adjacent the first sidewall and the second sidewall;

providing a second semiconductor layer over and adjacent the semiconductor structure;

performing a first directional implant of a first conductivity type of the second semiconductor layer from a first predetermined direction;

performing a second directional implant of a second conductivity type opposite the first conductivity type of the second semiconductor layer from a second predetermined direction that differs from the first predetermined direction;

~~forming a first current electrode region and a second current electrode region in the semiconductor substrate;~~

~~forming a second insulating layer adjacent the first sidewall and the second sidewall;~~

forming a conductive layer over the semiconductor structure and the second insulating layer; and

removing a portion of the conductive layer and the second semiconductor layer to ~~form~~ physically separate a first ~~electrode~~ gate region and a second ~~electrode~~ gate region, wherein:

the first ~~electrode~~ gate region is adjacent the first sidewall of the semiconductor structure and has the first conductivity type; and

the second ~~electrode~~ gate region is adjacent the second sidewall of the semiconductor structure and has the second conductivity type, the semiconductor structure preventing migration of doping species between the first gate region and the second gate region~~; and the first electrode region and the second electrode region are physically isolated from each other~~.

2. (Original) The method of claim 1 wherein the semiconductor structure is a channel region of the vertical double gate semiconductor device.

Claim 3 (Previously cancelled)

4. (Currently Amended) The method of claim 1 wherein removing the ~~portions~~ portion of the conductive layer and the second semiconductor layer comprises planarizing the second semiconductor layer and the conductive layer.

5. (Currently Amended) The method of claim 1 ~~wherein forming the conductive layer further comprises:~~

~~forming a second semiconductor layer; and~~

~~doping the second semiconductor layer in a first area adjacent the semiconductor structure with a first species~~ further comprising forming a first current electrode region and a second current electrode region in the semiconductor substrate to implement the vertical double gate semiconductor device as a transistor.

Please cancel claim 6.

7. (Currently Amended) The method of claim ~~6~~ 1, wherein ~~doping the second semiconductor layer~~ each of the first directional implant and the second directional implant is performed by ion implantation at ~~an angle~~ symmetric opposing angles relative to a top surface of the semiconductor substrate.

8. (Currently Amended) The method of claim ~~6~~ 1, further comprising annealing the first ~~electrode~~ gate region and the second ~~electrode~~ gate region after the first directional implant and the second directional implant ~~doping the second semiconductor layer~~.

9. (Currently Amended) The method of claim ~~6~~ 1, wherein removing a portion of the conductive layer is performed after doping the second semiconductor layer in a first area adjacent the semiconductor structure with a first species.

10. (Currently Amended) The method of claim ~~6, wherein the first area is part of the first electrode region and the second area is part of the second electrode region~~ 1 further comprising electrically coupling the first gate region and the second gate region.

11. (Currently Amended) The method of claim 1, further comprising forming a metal layer as the conductive layer ~~over the first electrode region and the second electrode region~~.

12. (Currently Amended) The method of claim 1, wherein forming the ~~metal~~ conductive layer comprises:

forming a silicon layer over the first ~~electrode~~ gate region, the second ~~electrode~~ gate region, and the semiconductor structure;

forming a first metal layer over the silicon layer; and

heating the semiconductor substrate so that the silicon layer and the first metal layer form a silicide.

13. (Currently Amended) The method of claim 12, further comprising: removing a portion of the ~~metal~~ conductive layer to form a first contact for the first electrode region and a second contact for the second electrode region, wherein the first contact and the second contact are electrically isolated from each other.

14. (Currently Amended) The method of claim 13, wherein removing a portion of the ~~metal~~ conductive layer comprises planarizing the conductive layer ~~metal~~.

15. (Currently Amended) The method of claim 11, further comprising annealing the first electrode region and the second electrode region before forming the metal layer.

16. (Currently Amended) The method of claim 11, wherein the metal layer further comprises ~~is~~ a stack of metal layers.

17. (Currently Amended) A method of forming a vertical double gate semiconductor device comprising:

providing a semiconductor substrate;

forming a first insulating layer over the semiconductor substrate;

forming a first semiconductor layer on the first insulating layer;

etching portions of the first semiconductor layer to form a semiconductor structure having a first sidewall and a second sidewall, wherein the first sidewall is opposite the second sidewall in a first direction;

forming a source region and a drain region ~~in~~ overlying the semiconductor substrate in a second direction, wherein the first direction is substantially perpendicular the second direction;

forming a second insulating layer on the first sidewall and the second sidewall;

forming a second semiconductor layer over the semiconductor structure and the second insulating layer, wherein the second semiconductor layer comprises:

a first semiconductor portion which is adjacent the first sidewall;

a second semiconductor portion which is over the semiconductor structure;

and

a third semiconductor portion which is adjacent the second sidewall;

doping the first semiconductor portion and the third semiconductor portion; and

removing the second semiconductor portion to physically separate the first semiconductor portion and the third semiconductor portion via the semiconductor structure to substantially eliminate migration of doping species between the first semiconductor portion and the third semiconductor portion, the semiconductor structure comprising differing material composition than the first semiconductor portion and the third semiconductor portion at all adjoining surfaces.

18. (Original) The method of claim 17, wherein the second insulating layer is deposited conformally.

19. (Original) The method of claim 17 further comprising annealing the second semiconductor layer.

20. (Original) The method of claim 19 wherein annealing is performed after removing the second semiconductor portion.

21. (Original) The method of claim 17 wherein removing the second portion is performed by a method selected from the group of anisotropic etching, planarization and etch back.

22. (Original) The method of claim 17 wherein doping the first semiconductor portion and the third semiconductor portion further comprises doping the first semiconductor portion with a first species and doping the third semiconductor portion with a second species, wherein the first species and the second species are different in conductivity.

23. (Original) The method of claim 17, wherein doping the first semiconductor portion and the third semiconductor portion is performed by ion implanting species at an angle relative to a top surface of the semiconductor substrate.

24. (Original) The method of claim 17, wherein doping the first semiconductor portion and the third semiconductor portion further includes forming a patterned layer over the semiconductor substrate.

25. (Original) The method of claim 17, wherein etching portions of the first semiconductor layer to form the semiconductor structure further comprises:

forming a third insulating layer over the first semiconductor layer;

forming a nitride layer over the third insulating layer;

patterning the nitride layer and the third insulating layer; and

etching the first semiconductor layer using the nitride layer and the third insulating layer as a mask.

Claims 26-33 (Previously Canceled)

34. (New) A method for forming a vertical double gate semiconductor device comprising:

providing a semiconductor substrate;

forming a semiconductor structure overlying the substrate and having a first sidewall and a second sidewall, wherein the first sidewall is opposite the second sidewall in a first direction;

forming an insulating layer on the first sidewall and the second sidewall;

forming a semiconductor layer over and around the semiconductor structure and the insulating layer, wherein the semiconductor layer comprises:

a first semiconductor portion which is adjacent the first sidewall;

a second semiconductor portion which is adjacent the second sidewall; and

a third semiconductor portion overlying the semiconductor structure;

doping the device with two angled implants of opposite conductivity type, the first semiconductor portion having a resulting first conductivity, the second semiconductor portion having a resulting second conductivity and the third semiconductor portion having mixed species doping; and

removing the third semiconductor portion to physically separate the first semiconductor portion and the second semiconductor portion via the semiconductor structure to substantially eliminate migration of doping species between the first semiconductor portion and the second semiconductor portion, the semiconductor structure comprising differing material composition than the first semiconductor portion and the second semiconductor portion at all adjoining surfaces.